

1 1. A method comprising:
2 receiving a processor identifier;
3 receiving a seed stored in a non-volatile memory;
4 and
5 hashing said identifier and said seed to develop
6 a device key.

1 2. The method of claim 1 further including
2 requesting a random number and hashing said identifier and
3 said seed with said random number.

1 3. The method of claim 2 including causing a
2 processor to execute instructions to obtain a processor
3 serial number.

1 4. The method of claim 1 including obtaining said
2 processor identifier by executing instructions at the
3 operating system kernel level.

1 5. The method of claim 2 including causing a
2 processor to obtain a random number from an integrated
3 circuit and generating a certificate.

1 6. The method of claim 5 including causing the
2 processor to send said certificate to said integrated
3 circuit.

1 7. The method of claim including causing said
2 integrated circuit to validate said certificate and process
3 said certificate to generate a device key.

1 8. The method of claim 7 including encrypting a new
2 device key using a current device key and writing the
3 encrypted new device key back to the processor.

1 9. The method of claim 7 including writing said
2 device key into a memory in said integrated circuit.

1 10. The method of claim 1 including receiving a
2 digital television broadcast from a head end and sending
3 said device key to said head end.

1 11. An article comprising a medium storing
2 instructions that enable a processor-based system to:
3 receive a processor identifier;
4 receive a seed stored in a non-volatile memory;
5 and
6 hash said identifier and said seed to develop a
7 device key.

1 12. The article of claim 11 further storing
2 instructions that enable the processor-based system to

3 request a random number and hash said identifier and said
4 seed with said random number.

1 13. The article of claim 12 further storing
2 instructions that enable the processor-based system to
3 execute instructions to obtain a processor serial number.

1 14. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 obtain said processor identifier by executing instructions
4 at ring 0.

1 15. The article of claim 12 further storing
2 instructions that enable the processor to obtain a random
3 number from an integrated circuit and generate a
4 certificate.

1 16. The article of claim 15 further storing
2 instructions that enable the processor-based system to send
3 said certificate to said integrated circuit.

1 17. The article of claim 16 further storing
2 instructions that enable the processor-based system to
3 cause said integrated circuit to validate said certificate
4 and process said certificate to generate a device key.

1 18. The article of claim 17 further storing
2 instructions that enable the processor-based system to
3 encrypt a new device key using a current device key.

1 19. The article of claim 17 further storing
2 instructions that enable the processor-based system to
3 write said device key into a memory in said integrated
4 circuit.

1 20. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 receive a digital television broadcast from the head end
4 and send said device key to said head end.

1 21. An integrated circuit comprising:
2 an interface to couple said circuit to a
3 processor-based system;
4 a transport demultiplexer coupled to said
5 interface to receive audio/video content information;
6 a key logic circuit to extract a device key from
7 a bit stream including a processor serial number and a
8 device key seed; and
9 a memory to store said device key.

1 22. The circuit of claim 21 wherein said memory is
2 part of said transport demultiplexer.

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1 23. The circuit of claim 21 including a bus that
2 couples said interface, said transport demultiplexer and
3 said key logic circuit.

1 24. The circuit of claim 21 wherein said key logic
2 circuit generates a random challenge on request from said
3 processor-based system.

1 25. The circuit of claim 21 wherein said key logic
2 circuit receives a certificate from said processor-based
3 system and processes said certificate to generate a device
4 key.

1 26. The circuit of claim 25 wherein said key logic
2 encrypts a new device key using a current device key.

1 27. A processor-based system comprising:
2 a processor that stores instructions that enable
3 said processor to obtain a processor serial number;
4 a non-volatile memory, coupled to said processor,
5 to store a device key seed;
6 an integrated circuit coupled to said processor,
7 said integrated circuit including a key logic circuit that
8 generates a random challenge upon request from said
9 processor.

1 28. The system of claim 27 wherein said key logic
2 circuit extracts the device key from a bit stream including
3 a processor serial number and a device key seed.

1 29. The system of claim 28 including a memory in said
2 integrated circuit, said key logic circuit enabling said
3 device key to be stored in said memory.

1 30. The system of claim 29 wherein said integrated
2 circuit includes a transport demultiplexer that receives
3 content from an external source, said memory being included
4 as part of said transport demultiplexer.

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